**Claim Status**

Claim 1. (Currently Twice Amended) A semiconductor package for three-dimensional mounting, comprising:

a first substrate having an upper surface on which a first metal pattern is formed and a lower surface on which a second metal pattern is formed, said first metal pattern and second metal pattern being electrically connected to each other;

a semiconductor chip which is placed on the upper surface of the first substrate and is electrically connected to the first metal pattern;

a sealing resin layer which is formed on the upper surface of the first substrate and seals the semiconductor chip and the first metal pattern;

a conductive wire which passes through the resin layer and has one end electrically connected to the first metal pattern and the other end exposed at a top surface of the resin layer, the exposed other end of said conductive wire and the top surface of the resin layer being substantially level with each other, the exposed other end of said conductive wire being adapted to receive a first solder ball directly thereon; ~~and~~

a first electrode which is formed on the lower surface of the first substrate and is electrically connected to the second metal pattern; and

a second solder ball directly bonded to said first electrode,

wherein when the first solder ball is received on the exposed other end of said conductive wire, the first solder ball will be disposed in alignment with said second solder ball, and said second solder ball will be electrically connected to the first solder

ball, thereby allowing said first substrate to be connected to another substrate, with said first substrate having a same orientation as the another substrate.

Claim 2 (Cancelled).

Claim 3 (Currently Once Amended): A semiconductor package according to claim 1, further comprising a second substrate placed ~~on~~ over the surface of the resin layer, having an upper surface and a lower surface opposite the upper surface, wherein the second substrate includes a third metal pattern which is electrically connected to the other end of the conductive wire from the lower surface of the second substrate, and a second electrode which is formed on the upper surface of the second substrate and is electrically connected to the third metal pattern.

Claim 4 (Currently Once Amended): A semiconductor package according to claim 3, wherein a solder ball is bonded to ~~at least one of the first electrode at the first substrate and~~ the second electrode at the second substrate.

Claims 5 and 6 (Cancelled).

Claim 7 (Original): A semiconductor package according to claim 3, wherein the first electrode and the second electrode are disposed at different positions in horizontal directions.

Claim 8 (Original): A semiconductor package according to claim 7, wherein a second semiconductor chip is stacked on the upper surface of the second substrate, the second semiconductor chip being electrically connected to the second electrode and having a function different from that of the semiconductor chip.

Claims 9 and 10 (Cancelled).

Claim 11 (Original): A semiconductor device in which the semiconductor package for three-dimensional mounting of claim 1 is mounted on a mother board.

Claim 12 (Original): A semiconductor device in which a plurality of semiconductor packages of claim 1 are stacked.

Claim 13 (Original): A semiconductor device according to claim 12, wherein semiconductor chips of the semiconductor packages of the plurality of semiconductor packages, comprise memory elements.

Claims 14-23 (Previously Cancelled).

Claim 24 (Currently Twice Amended): A semiconductor package for three-dimensional mounting, comprising:

a first substrate having an upper surface on which a first metal pattern is formed and a lower surface on which a second metal pattern is formed, said first metal pattern and second metal pattern being electrically connected to each other;

a semiconductor chip which is placed on the upper surface of the first substrate and is electrically connected to the first metal pattern;

a sealing resin layer which is formed on the upper surface of the first substrate and seals the semiconductor chip and the first metal pattern;

a conductive wire which passes through the resin layer and has one end electrically connected to the first metal pattern and the other end exposed at a top surface of the resin layer, the exposed other end of said conductive wire and the top surface of the resin layer being substantially level with each other;

a first electrode which is formed on the lower surface of the first substrate and is electrically connected to the second metal pattern; ~~and~~

a wiring pattern formed over the sealing resin layer and being electrically connected to the conductive wire, said wiring pattern being comprised of at least a first wiring and a second wiring, said first wiring being disposed closer to a center of the semiconductor package than said second wiring is, and said second wiring being disposed closer toward a periphery of the semiconductor package than said first wiring is,

wherein said wiring pattern comprises a plurality of said first wirings, and a plurality of said second wirings, said first wirings and said second wirings being alternatingly arranged.

Claim 25 (Previously Cancelled).

Claim 26 (Currently Once Amended): A semiconductor package for three-dimensional mounting, comprising:

a first substrate having an upper surface on which a first metal pattern is formed and a lower surface on which a second metal pattern is formed, said first metal pattern and second metal pattern being electrically connected to each other;

a semiconductor chip which is placed on the upper surface of the first substrate and is electrically connected to the first metal pattern;

a sealing resin layer which is formed on the upper surface of the first substrate and seals the semiconductor chip and the first metal pattern;

a conductive wire which passes through the resin layer and has one end electrically connected to the first metal pattern and the other end exposed at a top surface of the resin layer, the exposed other end of said conductive wire and the top surface of the resin layer being substantially level with each other;

a first electrode which is formed on the lower surface of the first substrate and is electrically connected to the second metal pattern;

a wiring pattern formed over the sealing resin layer and being electrically connected to the conductive wire, said wiring pattern being comprised of Cu; and

a second electrode formed on the wiring pattern, the second electrode including an Ni layer in electrical connection with the wiring pattern, and an Au layer disposed on the Ni layer.